Power consumption and costs analysis comparison on WBG-based active dv/dt filtering inverters

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*Abstract*— Wide-bandgap (WBG) active dv/dt filtering inverters are taking relevance in power electronics due to improvements in inverter design and power losses. Enabling high working frequency and so low rise time, WBG based inverters observe high voltage gradients (dv/dt). Different aspects in architecture design must be taken into account to reduce this drawback. In this paper, a trade-off between power losses restraint, voltage overshoot suppression and costs is presented comparing various inverter models and a proposed solution.

Keywords—SiC MOS, Reliability, Voltage Overshoot, dv/dt, PWM Inverter, PD, insulation degradation.

# Introduction

European standard known as “Stage V” imposes the reduction of internal combustion engine (ICE) size starting from 2020. In order to improve CO2 emissions, new components such as filters and fluids mixtures are mandatory in thermal motor design with pollution reduction as unique goal. This condition causes drawbacks in terms of space for ICE volume and even more complex architectures are requested. To overcome this problem, the electrification of automotive, industrial and agricultural vehicles is taking relevance [1]. Referring to the last group, agricultural tractors producers are moving to hybrid or full-electric vehicles design observing economical improvements compared to ICE tractors [2],[3]. This passage is permitted as electrification technology is improving in efficiency and final product costs. These two elements are dependent from different aspects as:

* Electric motor design material. In particular, in order to obtain electromagnetically efficient permanent magnets, rare earth materials represent the best choice. Costs are affected as the price of these materials is rising due to demand [4].
* Electric motor winding technology. New conductors design, such as hairpins, are improving secondary effects on current flow. Costs increases proportionally to copper density that is rising as conductor resistance must be lowered to permit high current density for power requirement [5].
* Electric motor thermal design. As power requirements increases, thermal dissipation is taking relevant role in efficiency, reliability and costs of machines [6].
* Inverter design. Improvements in current and voltage waveform generation for electric motor supply permit to reduces power losses at device level. This goal must be reached taking into account final costs of structure [7].

The final point for the improvements of efficiency and costs is treated in this paper. It is mandatory to consider a filtering action in architecture design. In fact, filtering of the output waveforms is mandatory to focus power generated to the desired harmonic frequency and to reduces voltage overshoots at electric motor inputs, i.e. dv/dt reduction. Passive filters, new winding insulation materials, form-wound windings and active filtering represent different solutions for this problem [7]. Active filtering is chosen here as it deals only with inverter design architecture instead of volume increments and devices additions requested by others solutions listed. For this choice, power consumptions and costs are related to device density and technology allowing power increment for electric motor. Nowadays, Wide Band Gap (WBG) semiconductors are taking relevance in place of IGBTs for reduced channel resistance and increased working frequency and so this is the technology adopted for all architectures proposed in this treatise. The efficacy of active filtering combined with WBG technology is proven with voltage overshoot suppression. The paper is structured in these sections: in chapter II inverter architecture are analysed in terms of devices disposition, in chapter III conduction and switching losses are computed and inverters are simulated with different current values, dc-link voltage and carrier frequency, phase to phase voltage overshoot for benchmark architectures is obtained, costs analysis is computed in chapter IV conclusions are taken.

# Inverter stuctures analysed

The analysed inverter structures, introduced in this section, are:

1. Two levels inverter (2-level),
2. Three levels Neutral Point Clamped NPC inverter (3-level),
3. Three levels T-type inverter (T-type),
4. Three levels inverter with voltage suppression (β-type),
5. Staggered multi-leg inverter (Multi-leg),
6. Multi-leg inverter with voltage suppression (proposed solution, PS).

First model is 2-level inverter, shown in Figure 1 with a single leg and voltage waveform and signals. It’s simplicity in realization is exploited for comparative study. Voltage pass directly from to (i.e. the DC-link voltage) and vice versa in a step function manner.

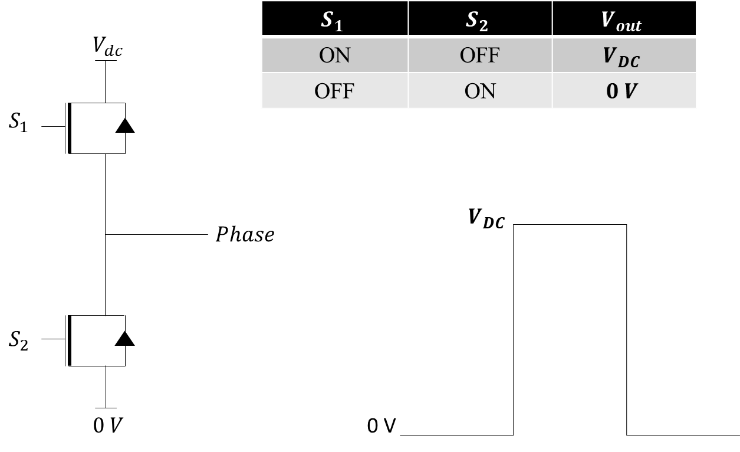


Figure 1 Single phase of the 2 level inverter

Second model is 3-level inverter shown in Figure 2. Adding 2 devices and the clamping diodes, during the positive half-wave, the output voltage switches between Vdc and Vdc/2, whereas commutation is between 0 and Vdc/2 during negative half-wave. Increasing the number of voltage levels, reduced dv/dt is obtained and harmonic content of output voltage waveform is reduced with respect to 2-level. Increased complexity, costs and power losses are the main drawbacks of this architecture.

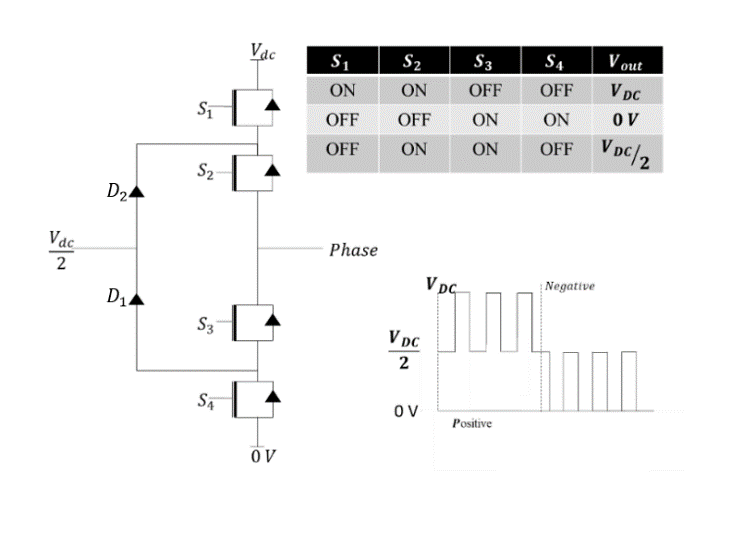


Figure 2 Single phase of 3-level inverter, positive and negative half period of output voltage wave

## Third model is T-type inverter, shown in Figure 3. This architecutre permits to obtain same voltage waveform as 3-level with lowered power losses [8]. Two devices per leg are added with antiparallel diodes to allow current flow in negative direction for in line transistors (S3 and S4) [9]. Lower complexity with respect 3-level is obtained. The unique drawback is related to conduction and switching stress applied to S1 and S2 as they need to sustain whole dc-link voltage.

## A picture containing graphical user interface Description automatically generated

Figure 3 Single phase of T-Type inverter, positive and negative half period of output voltage wave

Fourth model is β-type inverter, shown in Figure 4. As T-type, it represents a different solution to 2-level inverter adding two in line transistors, i.e. same number of devices as T-type [10].

Three voltage levels are obtained with voltage suppression concept introducing half dc-link voltage for a specific short time . In Figure 4, the output voltage stays at Vdc/2 for seconds and then, due to reflection of the wave, it passes at Vdc. Starting from the impedance of the cable, seconds is the delay experienced by the waveform along cables from inverter to Electric motor, where L and C are respectively the per meter inductance and capacitance of the cable; so . The reflected voltage waveform at motor terminal returns at inverter output with a delay of 2τ, i.e. . This phenomenon causes a phase delay of 2π for the voltage waveform reflected. Finally, another voltage transition is generated and the two waves constructively interfere dumping the resonance. Due to short delay time, assumes low values compared to whole switching period. This condition permits to avoid neutral point balancing experienced in three-level and it reduces costs for in line transistors as the third level does not carry any significant amount of current.

## 

Figure 4 Single phase of Beta inverter

Fifth model is the staggered switching inverter, shown in Figure 5. It is recalled Multi-leg [12]. The basic idea is to replicate 2-levl leg and to sum each single voltage waveform with interphase coupled inductors. The number of steps depends on the number of the legs activated in parallel in a staggered manner. The model in Figure 5 is the case with 4 legs per phase. It takes three different intermediate levels between 0 and Vdc. The staggered levels are spaced in time by β seconds as for β-type inverter. Legs are switched on with same β delay. The parallel of devices allows to reduce conduction losses dividing current.

## 

Figure 5 Single phase of Multi-leg inverter

In Figure 6, the last inverter architecture is shown. This model is a proposed solution obtained combining the β-type and the Multi-leg inverters. The basic idea is to exploit voltage suppression of β-type and parallel paths sum with coupled inductors of Multi-leg. Voltage waveform is equal to Multi-leg introducing β delay between steps. MOSFETS connected to S5 and S6 in Figure 6 need to sustain half dc-link voltage reducing final costs with respect to Multi-leg.

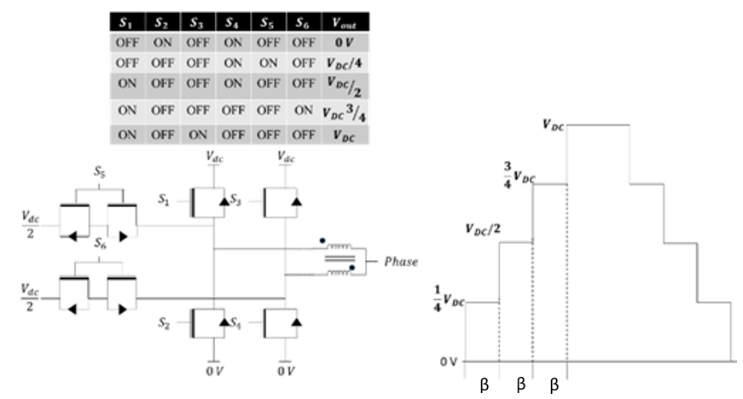


Figure 6 Single phase of the proposed solution

# Comparison of the analysed Architectures

## Power losses computation

A first comparative analysis is obtained computing conduction and switching losses. Similar approach as in [13] is applied to extract single device losses per type.

Considering a single leg of 2-level inverter, in Figure 1, S1 switch ON in the first half period, S2 is OFF; S1 switch OFF in the second half period and S2 switch ON. Conduction losses for 2-level is obtained in (1):

|  |  |
| --- | --- |
|  | (1) |

Where *i* is the inverter output current, *RDSon* the equivalent on-state resistance of the MOSFET model and *D* is duty cycle. In case of variable frequency drive, *i*=*Im*\*sin(*ωt+θ*), with Im the peak of the inverter output current, ω its angular frequency and θ the phase displacement between current and voltage.

For 3-level inverter in Figure 2, power consumption is the sum of MOSFETs and diodes. Recalling that for a single leg, clamping diodes and the middle devices (S2, S3) permits to set the output voltage to Vdc/2. The output voltage varies between Vdc and Vdc/2 during the positive half-wave and between 0 and Vdc/2 during negative half-wave. Conduction losses for external devices Pc\_ext are defined in (2), conduction losses for internal devices Pc\_int are reported in (3).

|  |  |
| --- | --- |
|  | (2) |
|  | (3) |

Each diode consumes in conduction as in (4), where the voltage drop across the devices is expressed as with threshold voltage depending on device technology.

|  |  |
| --- | --- |
|  | (4) |

For T-type inverter, shown in Figure 3, due to the lower number of devices in conduction when converter is forcing 0 and Vdc voltages, it improves conduction losses respect 3-level inverter. However, leg devices (S1 and S2) must sustain dc link voltage.Conduction losses for leg devices S1 and S2 are the same as in (2). For in line devices, i.e. S3 and S5, Pc\_int can be computed as in (5).

|  |  |
| --- | --- |
|  | (5) |

For β-type inverter, shown in Figure 4, conduction losses are similar to 2-level inverter. Conduction losses for a single Beta inverter’s device is different with respect T-type inverter due to the in line transistors control S3, in Figure 4, and is computed as (6):

|  |  |
| --- | --- |
|  | (6) |

For Multi-leg inverter in Figure 5, the devices that conduct in parallel are summed with coupled inductors cutting down losses. Referring to Figure 5, with 4 legs per phase, the time shift between levels is . Conduction losses computation can be simplified considering that current trough devices remains constant from seconds to . For a single device in Multi leg inverter, conduction losses are defined in (7):

|  |  |
| --- | --- |
|  | (7) |

For proposed solution in Figure 6, conduction losses are similar to (7). Here, current is not divided in four parallel paths but two. For proposed solution is defined in (8):

|  |  |
| --- | --- |
|  | (8) |

For the sake of completeness, switching losses are reported in (9) and (10), where and Im are the actual voltage and current values at which the device turns on and off, is the switching frequency, is the turn-on energy loss, is the turn-off energy loss. These last terms are available in datasheets of devices. are values obtained under test condition defined in datasheet of device.

## Efficiency Comparison

In order to obtain a fair comparison between architectures that require different current and voltage values, two models of Silicon Carbide (SiC) MOSFETs are used. The first transistor is a Littelfuse LSIC1MO120E0080, a 1200V class MOSFET (80 mΩ nominal RDSon) that sustains dc-link voltage. The second transistor has been chosen in order to observe same continuous drain current profile respect case temperature TC as the first one; it is Infineon IMW65R048M1H that sustains half dc-link voltage, i.e. up to 650V (48 mΩ nominal RDSon).

For each architecture, the number of devices as respective models is listed in Table 1.

Conduction and switching losses are simulated with PLECS imposing same boundary condition and current required as listed in Table 2.

Two different switching frequencies have been analysed, the nominal 20 kHz of the reference system and its double, 40 kHz, to investigate the possibility of exploiting more SiC fast commutation performance. Current value imposed is 20 A, with dc-link voltage that varies between 500 V and 800V.

*Table 1 Number of devices per architecture*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| MOSFET | 2-level | Beta-type | 3-level | T-type | Multi-leg | PS |
| 650V IMW65R048M1H | 0 | 6 | 12+6 diodes | 6 | 0 | 12 |
| 1200V LSIC1MO120E0080 | 6 | 6 | 0 | 6 | 24 | 12 |
| Coupled Inductors | 0 | 0 | 0 | 0 | 18 | 6 |

Table 2 Simulation Parameters

|  |  |
| --- | --- |
| DC Link voltage VDC | 500 – 800 V |
| Output Current I | 20 A |
| Switching frequency fSW | 10-40 kHz |
| Fundamental frequency of the modulated voltage fC | 50 Hz |
| Load Resistor Rload | 10 |
| Load inductor Lload | 1 |
| Series resistance for coupled inductors RCI | 1m |

Results are reported in Figures 7-10, where conduction losses are in green and switching losses in blue.

When the simulations are run with a current value equal to 20A (see Figure 7-Figure 10), conduction losses are much larger than the switching losses for all the investigated topologies. This is especially true at 10kHz (see Figure 7 and Figure 8), where the last two topologies, i.e. Multi-leg and the proposed inverters, have much better performance with significantly lower losses. This is associated to the fact that the current path is composed by the parallel of devices that drain current thus reducing conduction losses. It should be also noted that, at this switching frequency, the impact of a DC link voltage increase (from 500V of Figure 7 to 800V of Figure 8) is minimal. On the other hand, increasing the switching frequency from 10kHz (Figure 7 and Figure 8) to 40kHz (Figure 9 and Figure 10), the switching losses increase significantly. This is however not sufficient to completely even out the balance, as conduction losses still favour the last two architectures.

Given that the DC-link voltage does not affect the results significantly.

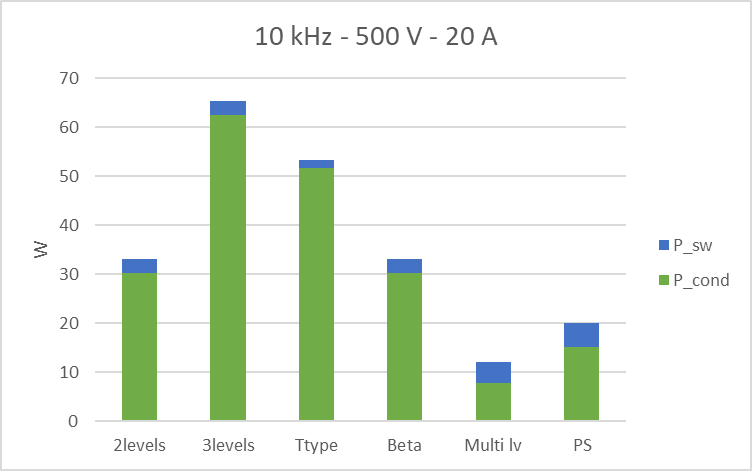


Figure 7 Conduction losses at 10k Hz 500 V and 20 A

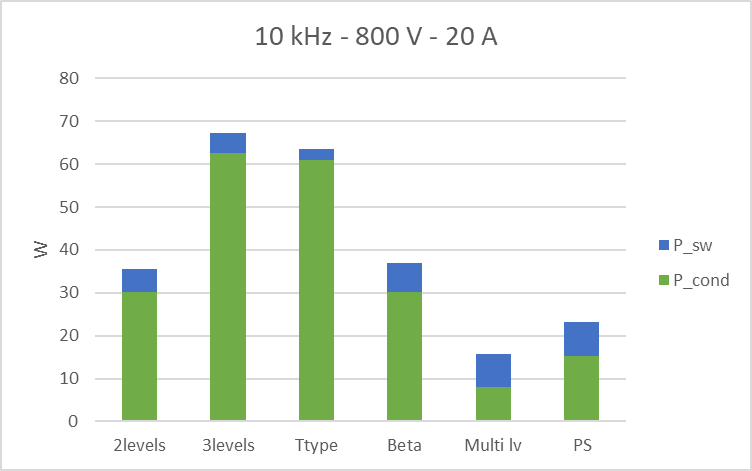


Figure 8 Conduction losses at 10k Hz 800 V and 20 A

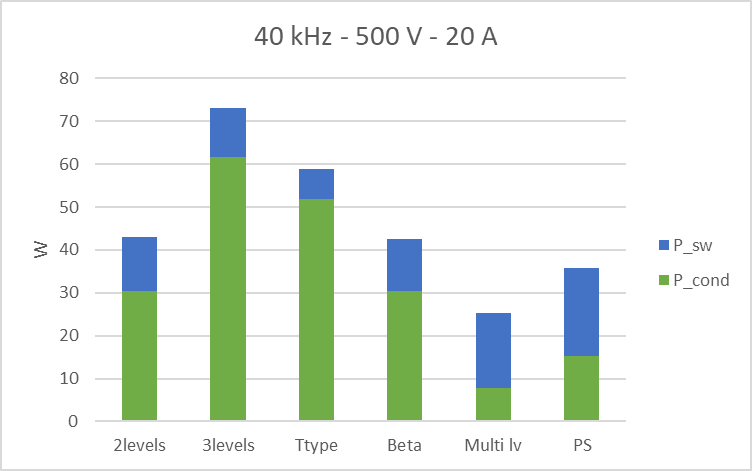


Figure 9 Conduction losses at 40k Hz 500 V and 20 A

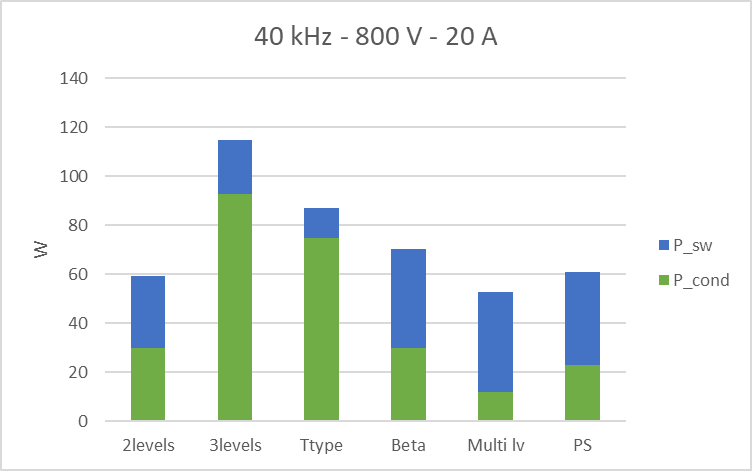


Figure 10 Conduction losses at 40 kHz 800 V and 20 A

## Phase to phase voltage overshoot

Due to the high working frequency introduced by WBG devices, the main drawback is voltage overshoot that increases as rise time is hugely lowered with respect to IGBTs. Increased number of levels to rise voltage from 0V to Vdc permits to improve this drawback. Simulations are performed with lumped element models of cables and EM obtained with MATLAB and Simulink. All parameters and values involved in simulations of architectures are listed in Table 3 studying phase to phase voltage overshoot.

Table 3 Overshoot analysis parameters

|  |  |
| --- | --- |
| Vdc | 500 V |
| Rise time | 25 -100 ns |
| Duty cycle | 50% |
| fsw | 40k Hz |

In Figure 11, 2-level, Beta, Multi-leg and Proposed solution inverters are compared with rise time equal to 100 ns [14]. 2-level suffers from the highest overshoot voltage while Multi-leg and Proposed solution observe same reduced overshoot.

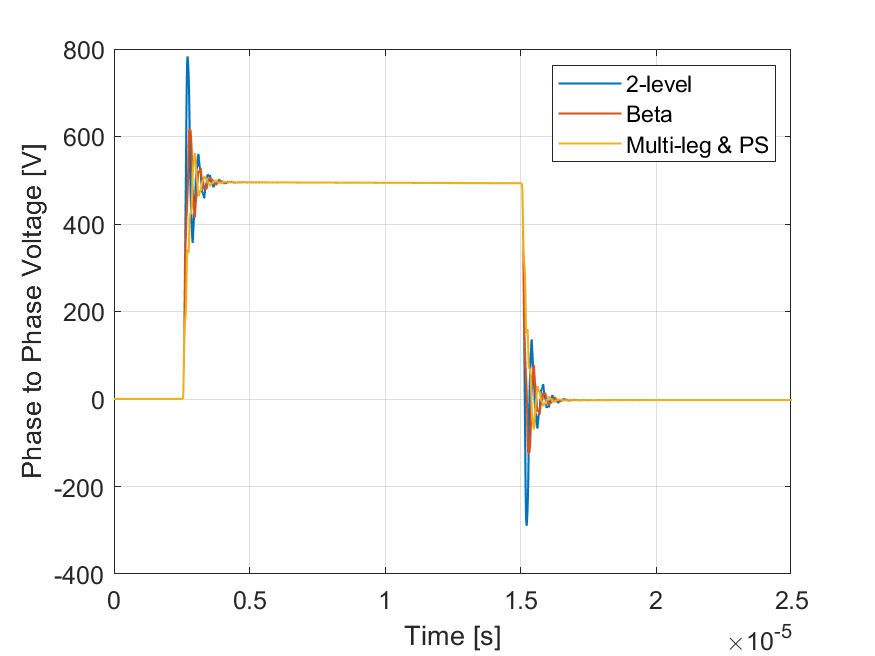


Figure 11 Phase-to-phase voltage overshoot with 100 ns rise time

In Figure 12, phase-to-phase voltage overshoot is studied with a rise time equal to 25 ns.

As rise time is reduced, 2-level and Beta inverters suffer from high voltage overshoots. Multi-leg and Proposed solution observe massive improvements with respect to the previous mentioned architectures allowing the usage of short rise time improving harmonics distortion too.

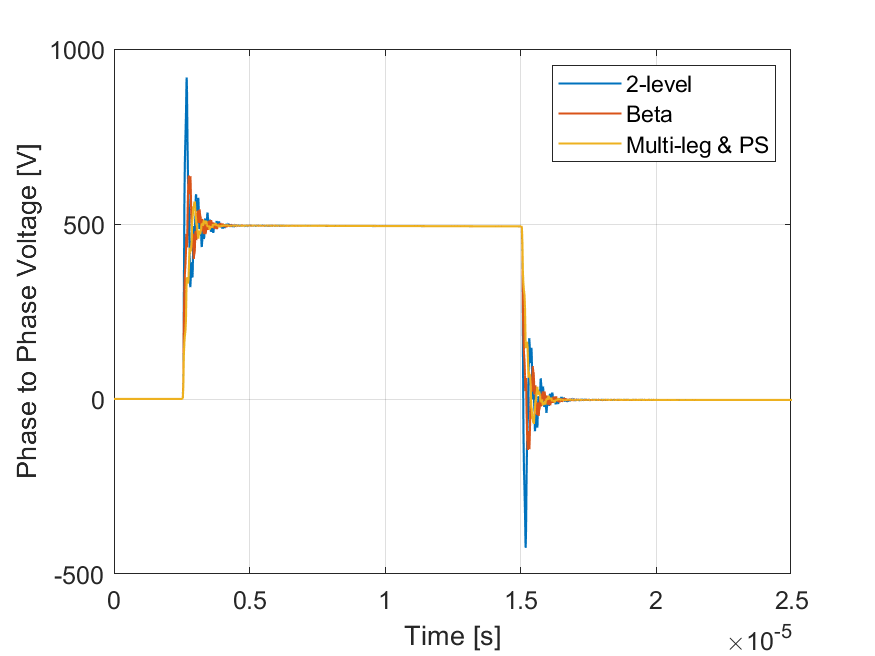


Figure 12 Phase-to-phase voltage overshoot with 25 ns rise time

For comparative analysis, maximum voltage overshoot at 100 ns rise time and 25 ns is listed in Table 4. As mentioned above, 2-level inverter voltage overshoot observes an increment of 136 V, Beta-inverter observes an increment of 29 V, Multi-leg and PS observe a variation of just 3 V. The property of voltage overshoot suppression is strictly related to reliability of the system [14].

Table 4 Maximum voltage overshoot at 25 ns and 100 ns rise time

|  |  |  |
| --- | --- | --- |
|  | RT=100 ns | RT=25 ns |
| 2-level inverter | 916 V | 780 V |
| Beta inverter | 632 V | 603 V |
| Multi-leg & PS inverter | 528 V | 561 V |

## Cost Aanalysis

To complete the study, a cost analysis needs also to be performed as it plays a role of paramount importance for the final decision [15]. It is important to underline that this comparison is not done to obtain an exact definition of the price, however it can still give valuable insight in the relative relationships among the various architectures.

For any power converter, the component with the biggest impact on the overall cost is the power device itself, especially when considering WBG devices. For the 2-level, 3-level, T-type and Beta inverters, the final cost is affected just by devices. For the staggered switching and Multi-leg inverters, the final cost is increased also by the inductors. The generic formula used for the calculation is as in (11).

Here, , and are the numbers of IMW65R048M1H and LSIC1MO120E0080 devices respectively, and are the costs-per-ampere of IMW65R048M1H and LSIC1MO120E0080 devices respectively, *P* is the packaging cost-per-device, *a* and *b* are physical size parameters, and are the copper and iron material weights respectively. The values for and have been obtained observing the price of both types of devices used and extrapolating the angular coefficient of the curve price, in € per 1000 units and per ampere. All parameters related to inductor and package cost are defined in [16]. The values of the quantities involved in (11) are reported in [15], whereas the results of the cost analysis are shown in Table 3. The 2 level and 3 level inverters represent the cheapest solutions. The β-type and T-type inverters have higher costs. In particular, they cost the same as they feature the same number of elements. A significant increase in costs is observed in the staggered switching and multi-leg cases. In particular, the former is by far the most expensive due to the higher number of elements involved.

Table 5 Parameters used for the cost analysis

|  |  |
| --- | --- |
| Parameter | Value |
| σ600 [€/A] | 0.56 |
| σ1200 [€/A] | 0.38 |
| P [€/unit] | 0.55 |
| Wcopper [kg] | 1.04 |
| Wfe [kg] | 0.03 |

Table 6 Number of devices per architecture for cost analysis

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Model | 2-level | Beta | 3-level | T-Type | Multi-leg | PS |
|  | 0 | 6 | 12 | 6 | 0 | 12 |
|  | 6 | 6 | 0 | 6 | 24 | 12 |
| Cost (€) | 75.252 | 124.15 | 97.8 | 124.15 | 930.73 | 458.21 |

# Conclusion

In this paper, six different WBG-based dv/dt active filtering inverters have been compared in terms of conduction and switching losses and costs. Active filtering plays the key role as cost effective choice permitting to avoid to increase complexity and so costs of architectures still allowing voltage overshoot restraint. As demonstrated, a trade-off between power losses and price is present. Observing results obtained from both analytical computations and simulations and the economical comparison obtained in the formal manner expressed in chapter III, the proposed solution reported in this treatise represents the optimal meeting point between these requirements. To enforce this sentence, phase to phase voltage overshoot is simulated for architectures observing remarkable advantages with proposed solution. Suffering from higher losses compared to Multi-leg inverter only, the proposed solution permits to obtain all benefits coming from multi-level inverters, even more levels than 3-level, T-type or Beta, with half the final price of the staggered switching inverter. Even if complexity of the architecture is increased with respect to 2-level and Beta inverters, the efficiency of the electric source is remarkably improved. Finally, looking at the complete system of electric motor and driver, this paper permits to convince more to the electrification of motor in above mentioned vehicle fields showing improvements in inverter section.

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